A 90-nm CMOS Quadrature Power Amplifier With High Efficiency Designed For Wireless Application

Dr. Luqman S. Ali luqmansufer@yahoo.com
Shamil H. Hussein Shangh1990@yahoo.com
Ahmad A. Ismail aismil1969@yahoo.com
Electrical Engineering .University Of Mosul
Mosul , Iraq

Abstract

The quadrature power amplifier (QPA) is used in a CMOS radio frequencies (RF) amplifier for wireless communication system such as WLAN and mobile communication (W-CDMA). Because of its high efficiency at high frequency operation and good linearity. This paper presents a design and analysis in the time and frequency domains for quadrature power amplifier based on 90-nm CMOS technology. The Class D power amplifier is used in the QPA configuration, because of the switch mode amplifiers provide amplification for modulated signals at RF with high efficiency and linearity. The quadrature signals are to be directly amplified by using a QPA without decomposing these signal to a phase and amplitude signal because of the lack of its separate avoid and the linearity and bandwidth requirements, thus reducing power consumption.

The results obtained show that the QPA can be used in a wide band spectrum. The amplifier has very good power added efficiency (PAE%) about (70.5%) and IDM3 is (-62.6dBm) at maximum output power (24.35dBm) and input power greater than (20dBm). The amplitude distortion has been obtained in this work about (1.36 dB/dB), and phase distortion about (0.27 degree/dB).

Keyword : Quadrature power amplifier(QPA), Quadrature modulator, classes amplifier.

استخدام تقنية (90-nm CMOS) لتصميم مكبر القدرة نوع(Quadrature) بكفاءة عالية في التطبيقات اللاسلكية

د. لقمان سفر علي شامل حمزة حسين احمد عبد الجبار اسماعيل
قسم الهندسة الكهربائية / جامعة الموصل

الخلاصة

يستخدم مكبر القدرة نوع (Quadrature) في التطبيقات اللاسلكية مثل (WLAN) وانظمة الاتصالات الخلوية (WCDMA) بسبب كفاءته العالية عند الترددات العالية وبخطية جيدة. تم في هذا البحث تصميم وتحليل بالحيزين الزمني والترددي لمكبر القدرة نوع (Quadrature) وبتقنية (90-nm CMOS). استُخدم في بناء المكبر مكبر القدرة نوع (D) لان مكبرات القدرة المفتاحية قادرة على تكبير الاشارات المضمنة عند الترددات الراديوية وبخطية جيدة وبكفاءة عالية. تم تضمين وتكبير اشارة المعلومات بشكل مباشر من خلال المكبر المستخدم بدون تفكيكها الى اشارة الاتساع واشارة الطور لان ذلك يوفر عرض حزمة واسعة وخطية عالية وقدرة استهلاك قليلة. تبين من خلال النتائج ان المكبر يعمل على طيف واسع من الترددات، وتمتلك خطية جيدة وكفاءة عالية حيت وصلت كفاءة القدرة المضافة الى حوالي(70.5%) وقيمة التداخل مع التوافقية الثالثة حوالي (-62.6dBm) عند اعظم قدرة اخراج (24.35dBm) وبقدرة ادخال اكبر من(20dBm). تم الحصول على اقل قيمة ممكنة لمقدار التشويه التي تشمل التشويه الاتساعي حوالي (1.36 dB/dB) والتشويه الطوري حوالي (0.27 degree/dB).

Received: 26 – 5 - 2015 **Accepted: 7 – 12 - 2015**

1- Introduction

The RF Power Amplifiers (PAs) are used in a wide variety of applications including wireless communication, TV transmissions, radar and RF heating. The basic techniques for RF power amplification can use classes as A, B, C, D, E, and F, for frequencies ranging from very low frequency through microwave frequencies. It is a critical element in transmitter units of communication systems, is expected to provide a suitable output power can range from a few mW to MW, depend by application. The output power from a PA must be sufficient for reliable transmission with a very good gain, high efficiency and linearity. High gain reduces the number of amplifier stages required to deliver the desired output power and hence reduces the size and manufacturing cost. High efficiency improves thermal management, battery lifetime and operational costs. Good linearity is necessary for bandwidth efficient modulation [1].

The mobile communication has become quite common in today with the increasing needs of effectively utilized bandwidth, and efficient and compact device technologies. The growth of wireless technologies is extremely fast. The information can be easily communicated by mobile communication system such as third generation wide-band code multiple access(W-CDMA). High efficiency and good linearity are among the important characteristics of a base station power amplifier used in plurality of the communication application. The PAs are typically blocks of radio frequency front end circuits, which take more care to get efficient PA for saving the power consumption [2].

In the RF transmitter, the message signal undergoes several steps such as digital signal processing, digital to analog conversion and filtering. The last step between up conversion of the baseband signal to RF frequencies and the antenna is the amplification of the signal. The conventional way of designing PA's is not to achieve maximum power transfer, but aiming for high efficiency and high linearity [3].

The power amplifier efficiency is a significant issue for the overall efficiency of most wireless system. Therefore, currently there are different kinds of Switched mode power amplifiers developed showing very high efficiency at higher frequencies. But all of these amplifiers are subjected to drive with the constant envelope signals. Whereas, for the increasing demand of high data rate transmissions in wireless communication there are some new modulation schemes introduced with generating no more a constant envelope signal but a high peak to average power signal. Therefore, recently a new technique is proposed, called the quadrature modulation for operating the switched mode PAs efficiently while driven by a high peak to average power signal [4].

C.H. Li et al. [5] presented a proposed of new power amplifier (PA) architecture as a more power efficient way to amplify modulated signals at radio-frequencies (RF) compared to conventional polar power amplifiers such as the Envelope Elimination and Restoration (EER) linearizing technique. the quadrature PA designed based on 90-nm CMOS models. They show a functional quadrature PA model with a power added efficiency of 30% at 6.4dBm output power driven at 2.4GHz and a maximum input power at 10MHz bandwidth, and 25% PAE at 5.1dBm output power at 50MHz. But the quadrature PA was designed in this paper has a good PAE about 70.5% at maximum output power of (24.35dBm) and input power greater than (20dBm) compared with [5].

In [6] F. Wang and others provided a detailed the wideband envelope elimination and restoration power amplifier(EER) with high efficiency wideband envelope amplifier for WLAN 802.11g applications. The authors have been gotten a PAE about 28% at 19dBm maximum output power driven at RF frequency 2.4GHz.

In this work an advanced design system (ADS) software has been used to design the RF amplifier type quadrature PA with high linearity and efficiency based on 90-nm process. The results obtained are very good and can be used on other frequencies such 2.14GHz for mobile communication and 2.45GHz for wireless applications

2- Quadrature Power Amplifier (QPA)

The QPA is a new power amplifier architecture and proposed as a more power efficient way to amplify modulated signals at radio-frequencies compared to conventional polar PAs. The quadrature signals as represented message signals (I(t) and Q(t)) can be directly amplified and modulated with RF carrier signal by using a QPA without decomposing the signal to phase and amplitude sets. The lack of a separating phase and amplitude signal path avoids the linearity and bandwidth requirements [5].

2-1 Quadrature Signals

The modulated RF signal is described as:

$V_{RF}(t) = A(t)\sin(\omega t + \varphi(t))$ ..... (1)

But written as

$V_{RF}(t) = A(t)\cos(\omega t + \varphi(t))$ ..... (2)

$V_{RF}(t) = A(t)[\cos(\omega t)\cos(\varphi(t) - \sin(\omega t)\sin(\varphi(t)]$ ..... (3)

$I(t) = A(t)\cos(\varphi(t))$ ..... (4)

$Q(t) = A(t)\sin(\varphi(t))$ ..... (5)

By using $I(t)$ and $Q(t)$ in the equation (3) resulting in:

$V_{RF}(t) = I(t)\cos(\omega t) - Q(t)\sin(\omega t)$ ..... (6)

This result shows that a modulated RF signal can also be expressed as a subtraction of two modulated quadrature signals I(t) and Q(t). Figure (1) shows a possible block diagram of such quadrature modulator scheme. Two message signals, I(t) and Q(t) are mixed with a local oscillator with a 90° phase shift with respect to each other. A subtraction is used to obtain the signal according to (6)[7]. Figure (2) shows the concept for a PA system. The most basic form consists of two quadrature modulated PA's, 90° phase difference in bridge mode. Each PA is driven by constant amplitude, constant phase, carrier signal with the voltage supply modulated by either I(t) or Q(t) signal. The load is an antenna sensing the difference between the modulated outputs of both PAs.

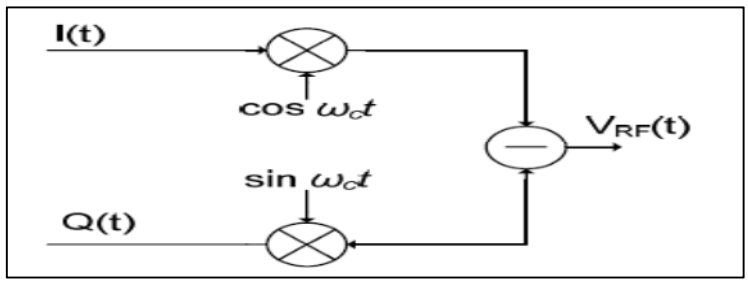


Figure (1): Quadrature modulator

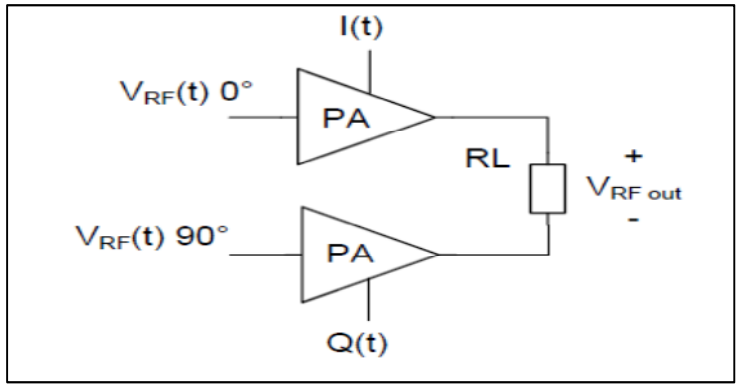


Figure (2): Block diagram of quadrature power amplifier

The bandwidth of the signal in a quadrature PA system, determined by the quadrature signals I(t) and Q(t), is much higher than the limited bandwidth of the other RF power amplifiers.

The downside of using a quadrature configuration is the mismatch between the I and Q side in amplitude or phase. The result is a corrupted reconstruction of the RF message signal, downgrading overall performance[8]. A second downside using a quadrature configuration is the need for a power combiner.

2-2 Choice Of PA Configuration In Quadrature PA System

The PA modulates an RF carrier signal with the quadrature signals I(t) and Q(t). The simplest way to achieve this is to use a switch mode amplifier such as Class D or Class E. These configurations are easily suitable for supply voltage modulation. Driving the amplifier with a hard switching RF signal and using the quadrature signal as supply voltage should generate the wanted modulated RF signal. Supply modulation using a linear mode amplifier such as Class-A or Class AB, would be impossible since the output current is not a direct and linear function of the voltage supply. Modulating and driving such PA configuration would involve a more complicated configuration [6].

The Class D has been choice in this work because of its higher efficiency, and it's a switch drive with a hard switching, 2.4-GHz, 50% duty cycle, RF pulse signal and the supply is connected to V_{DD}=1.2V. The output across the load RL between the nodes V_{out_I} (A-point) and V_{out_Q} (B-point) should be a sinusoid with constant amplitude of ($\sqrt{{V_{DD}}^2 + {V_{DD}}^2}$). And the Class D have a voltage source characteristic. A nett-current can flow back to the voltage supply and will not encounter the problems in Class E power amplifier (current source characteristics). In other words, a Class D will be suitable to operate in bridge mode for a quadrature PA system. The result is a switching modulating amplifier configured for modulation signals between V_{DD} and V_{SS}. The driving RF signal is now a function of the sign of the quadrature signal I(t) and Q(t). For a positive signed, the RF signal switches between zero and V_{DD}, for negative signed, between V_{SS} and zero. Figure (3) shows the output at node V_{XI}, node V_{XQ} of QPA and shows a modulated pulse signal for the full range of I(t) and Q(t). The LCR network will pass the fundamental tone as operate 2.4-GHz. The output is an amplitude modulated sinusoid waveform [4].

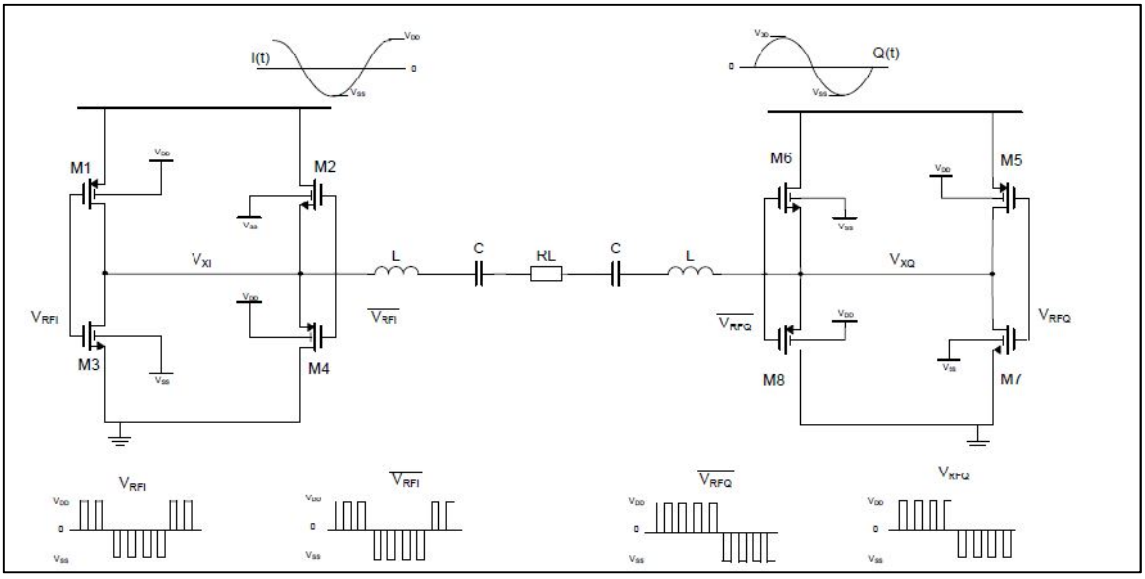


Figure (3): Quadrature power amplifier

3- Active Load Pull

And Source Pull Technique

The active load pull technique is based on the principle that applying current from a second phase coherent source that can vary the resistance or reactance of a RF load. This defies the usual understanding that RF loads are physically passive entities. The following analysis explains the concept as presented by Cripps in [2]. According to circuit theory, generator 1 sees a load resistance of R_L when generator 2 is set to supply zero current as shown in Figure (4). If generator 2 starts to supply current while generator 1 is set to zero, the voltage appearing across the load resistor can be given as:

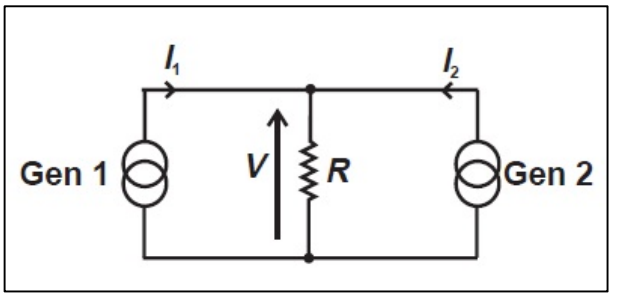


Figure (4): Active load pull schematic

$$V_L = R_L[I_1 + I_2] \quad \text{..... (7)}$$

Where V_L is the output voltage across output resistance (R_L) of the circuit design, I_1 and I_2 are currents draw from source and load of the design respectively. With the addition of supply current to the load resistance from second generator, the resistance seen by generator 1 now becomes. The input resistance (R_1) of the matching circuit can be represented by equation (8) with apply load current (I_2) to the load resistance (R_L).

$$R_{1=}R_L[\frac{I_1+I_2}{I_1}] \quad \text{..... (8)}$$

Likewise, the resistance seen by output matching circuit (R_2) can be represented as:

$$R_{2=}R_L[\frac{I_1+I_2}{I_2}] \quad \text{..... (9)}$$

The above concept can be extended to ac circuits by using complex notation for representing the magnitude and the phase of the currents and voltages and the resistive and reactive components. Thus, the equation (9) can be represented as:

$$Z_1 = R_L\left(1+\frac{I_1}{I_2}\right) \quad \text{..... (10)}$$

Where Z_1 is the impedance transformations (complex) of the matching circuit for RF design. It can be transformed to higher value if (I_2) is made in phase with (I_1) and to a smaller value if (I_2) is made anti-phase with (I_1). The concept of load pull technique can be implemented with transistors if the generators are replaced by the output trans-conductance of the RF transistors. Thus, when two transistors are connected in parallel, one can modify the impedance seen by the other through proper biasing. This concept, extended to the combination periphery and biasing, results in the quadrature configuration.

4- Simulation Results

The QPA and driver model is designed in 90nm CMOS technology operating at voltage modulated supply V_{DD}=1.2V and V_{SS}=-1.2V. Besides the 90nm feature length devices (channel length of the gate of all transistors L=90nm), larger devices models with a feature length of (L=240nm) were used, but the channel widths (W) depended on the fabrication area process. The QPA used in the wireless applications such as WLAN (IEEE 802.11 Standard)

that requires RF carrier frequency f_{RF}=2.4-GHz and mobile communication systems. The simulation of a design was performed by using ADS update 2009. Various procedures involved in the design of the QPA amplifier such as DC simulation, bias point selection, source and load-pull characterization, input and output matching circuit design and the design of suitable harmonic traps are explained.

4-1 Design Specifications

As mentioned earlier, WLAN requires high linearity to provide bandwidth efficiency. The QPA amplifier was designed to operate in the WLAN band (2.4 GHz) and was expected to meet the set of specifications listed in Table 1.

Table 1. Design specifications of power amplifier for WLAN

Operational center frequency (GHz)	2.4
Band Width Per Channel (MHz)	5-50
Maximum Output power (dBm)	20-26
PAE at maximum output power (%)	> 50 or better
Third order intermodulation products at maximum output power (dBc).	-20
Third order intermodulation products at 6dB back-off from maximum output power (dBc).	-30

4-2 Bias Point Simulation

The first step towards designing the QPA amplifier was to select a suitable bias point for operation. An amplifier can be biased as a Class A, AB, B or C amplifier and then suitable harmonic terminations can be designed to get efficiency higher than what could be achieved originally. In order to determine the bias point a DC bias point simulation was performed.

4-3 Load Pull And Source Pull

Load pull is a technique wherein the load impedance seen by the device under test (DUT). DUTs is varied and its performance is simultaneously measured [7]. Similarly in source pull the performance of the DUT for varying source impedances is measured. The measured results are very useful in determining the optimum load and source impedances which the device must see to give the best performance. Load pull, in particular, is commonly used to determine the load impedance required for maximizing efficiency. The input of a power amplifier is usually conjugate matched and the source pull is not always required [8]. It should be noted that the calculated impedance values vary with bias. In this design load pull and source pull were performed to obtained maximum efficiency. The results obtained from these simulation show the optimum value of load impedance is equal to (14.771+j*13.34) Ohm as shown in Figure (5).The output load equal to 50 Ohm. For transmitting maximum power because the matching between the output impedance of QPA and load 50 Ohm is done. Figure (6) shows the optimum value of input impedance of QPA is equal to (25.35+j*21.878) Ohm for transmitting maximum power because the matching between the input impedance and source 50 Ohm.

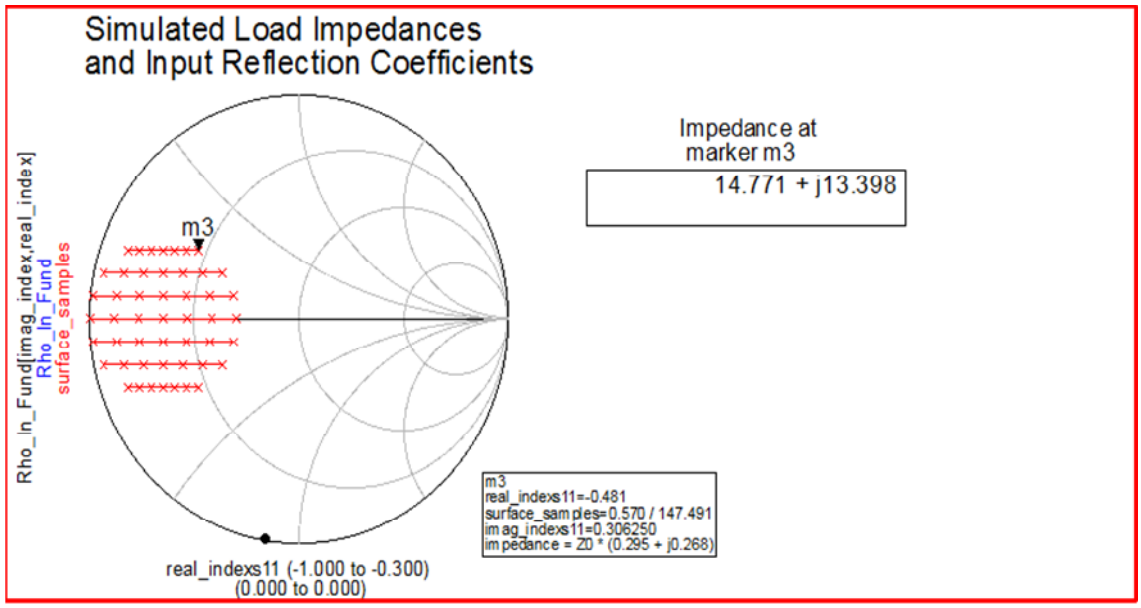


Figure (5): Load pull analysis to determine load impedance for maximum efficiency

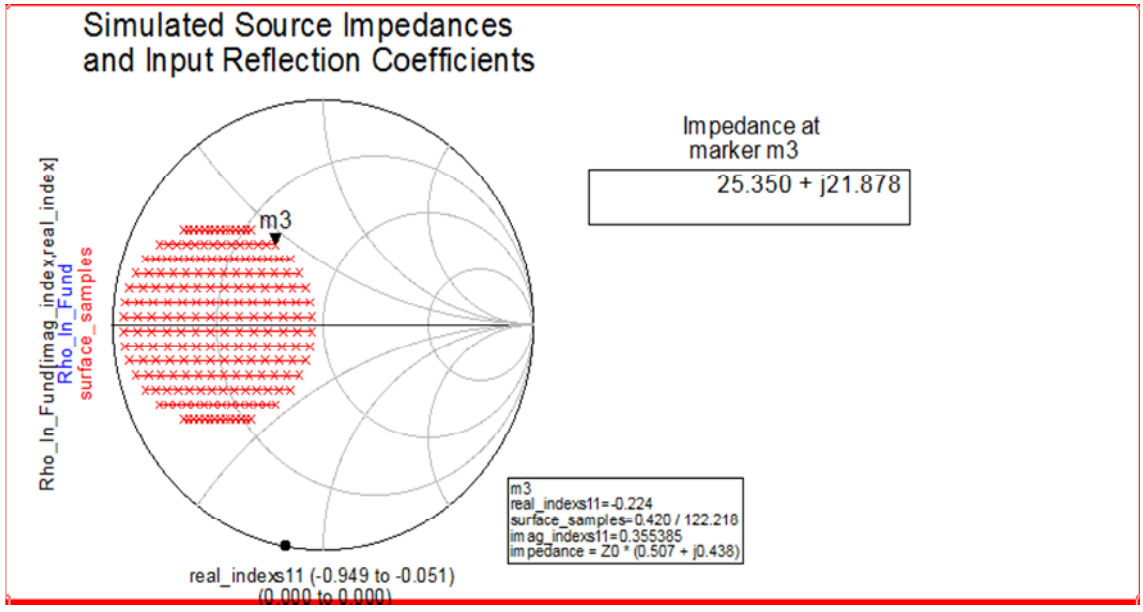


Figure (6): Source pull analysis to determine input impedance for maximum efficiency

4-4 Design Architecture Of Quadrature Power Amplifier

Figure (7) shows the basic architecture design of the QPA power amplifier. The QPA designed has been divided in to two power amplifiers (I-PAs and Q-PAs).

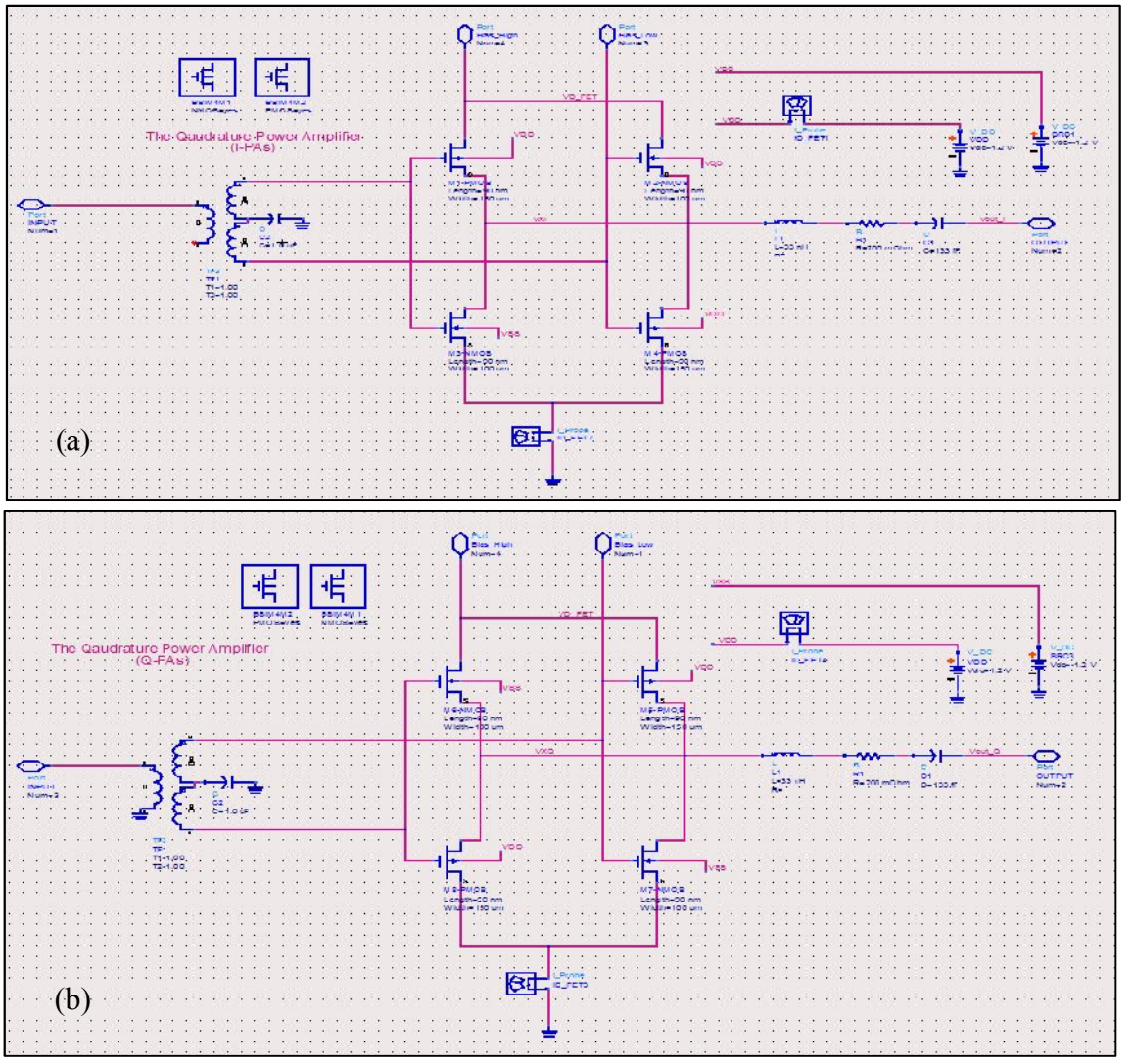


Figure (7): Single end of cmos quadrature PA. (a) I_PAs, (b) Q_PAs

4-5 Input And Output Matching

Input and output matching can be provided using simple discrete element matching network such as an L-match, T-match or π-match. An L-match was used in this work to output matching between output impedance (14.771+j*13.4)Ohm and load 50 Ohm. The input matching was used between input impedance (25.3+j*21.878) Ohm and source 50 Ohm. The quality factor (Q) of the tuned output network, sufficient for determine elements of matching circuits was choice about 10. Because of too low Q can result in a low suppression of the higher harmonics, a too high Q can result in large inductor values resulting in lower power

efficiency, a smaller load is 50 Ω and the output signal has been gotten is sinusoidal without amplitude and phase distortions. Figure (8) shows the schematic diagram of input matching and output matching of the QPA utilizing L-match network. Figure (9) represents the results of these matching via through input and output reflection coefficients (S_{11}),(S_{22}) respectively.

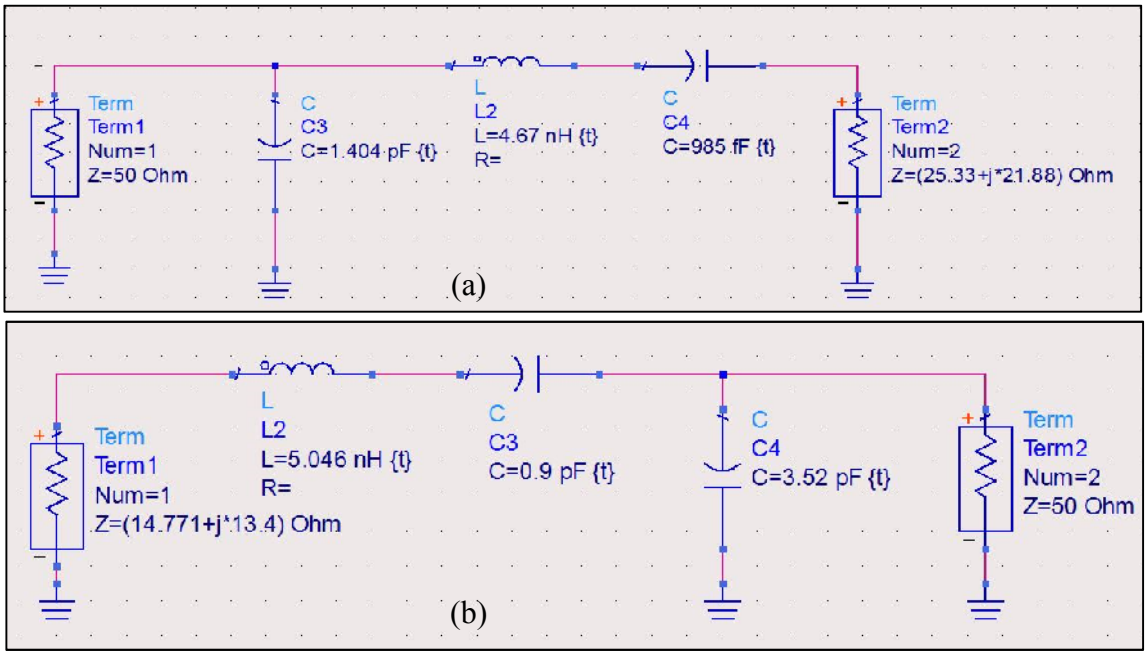
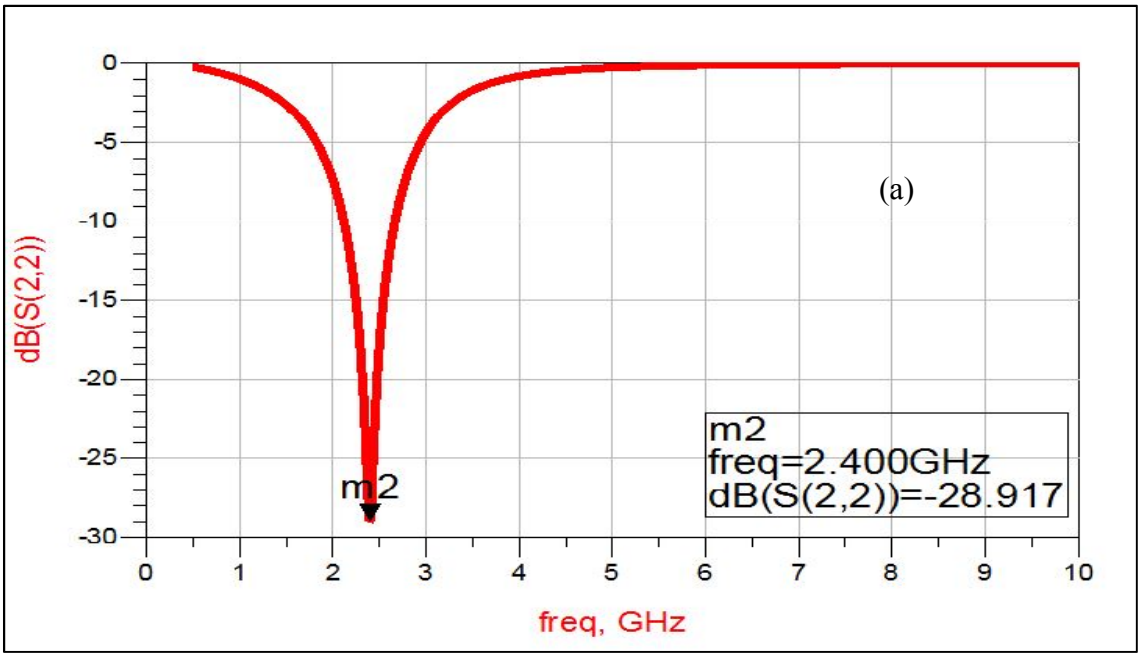


Figure (8): (a) Input matching of QPA, (b) Output matching of QPA



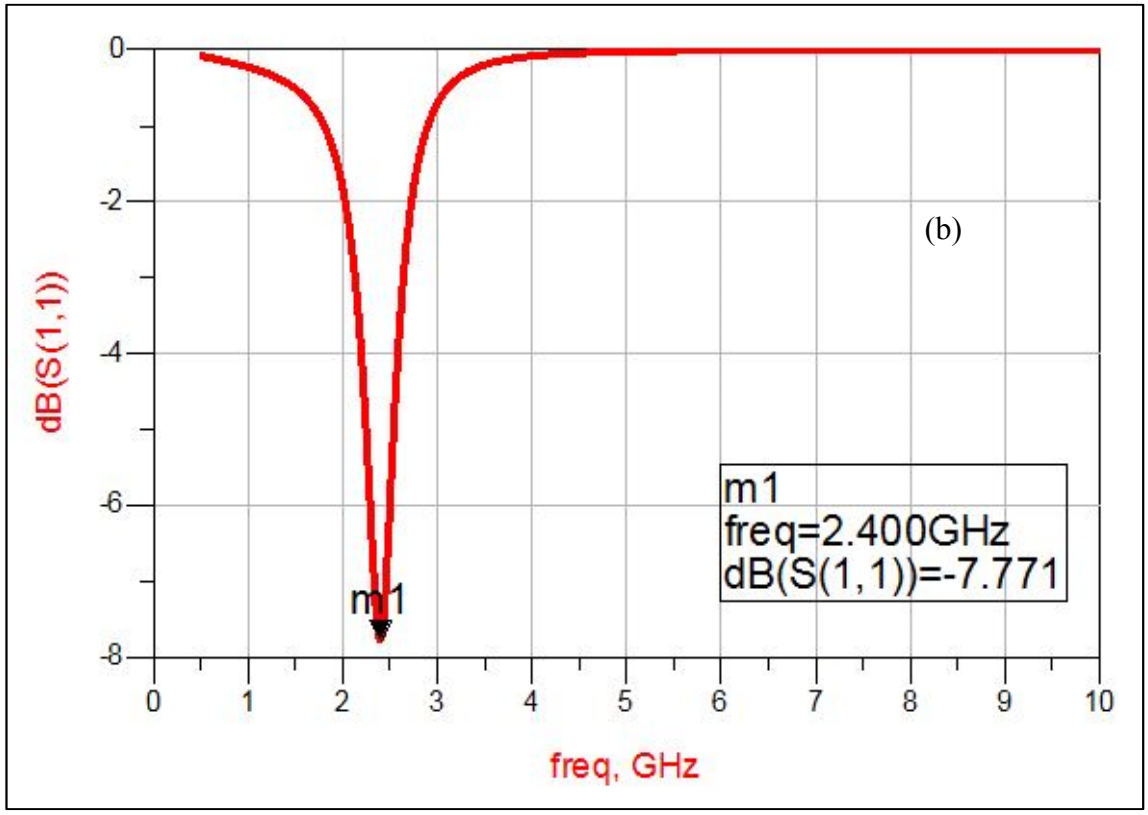


Figure (9): (a) Results of the input matching of the QPA (output reflection coefficient)
(b) Results of the output matching of the QPA (input reflection coefficient)

4-6 Design issues of a quadrature PA driver

The quadrature PA is driven by a hard switching RF signal pulse signal which will be positive or negative depending on the sign of the quadrature signal I(t). When I(t) is positive the RF signal will be a pulse signal switching between zero (ground) and V_{DD}. If I(t) is negative signed, the RF signal will switch between V_{SS} and zero (ground). To obtain such a signals, a possible driver topology is constructed as shown in Figure (10). The driver circuits consists of a chain of inverter output stages and two set of switches (transistors with channel length L=90nm). A quadrature signal parity bit SI(t), drives the two set of switches; one switches between V_{DD} and zero (ground) and the other between V_{SS} and zero (ground). The parity bit signal SI(t) is equal to V_{SS} when I(t) is signed positive and is equal to V_{DD} when I(t) is signed negative. An equivalent parity bit SQ(t) is assigned to the quadrature signal Q(t). The output of these sets of switches function the supply rails for the chain of inverters. The effects of this unbalanced driver output results in an uneven output for a single end quadrature PA, since its output is a direct function of the duty cycle. Conventionally, by changing the size of the transistors, the rise and fall times can be set in such a way that a duty cycle of 50% can be approximated [5].

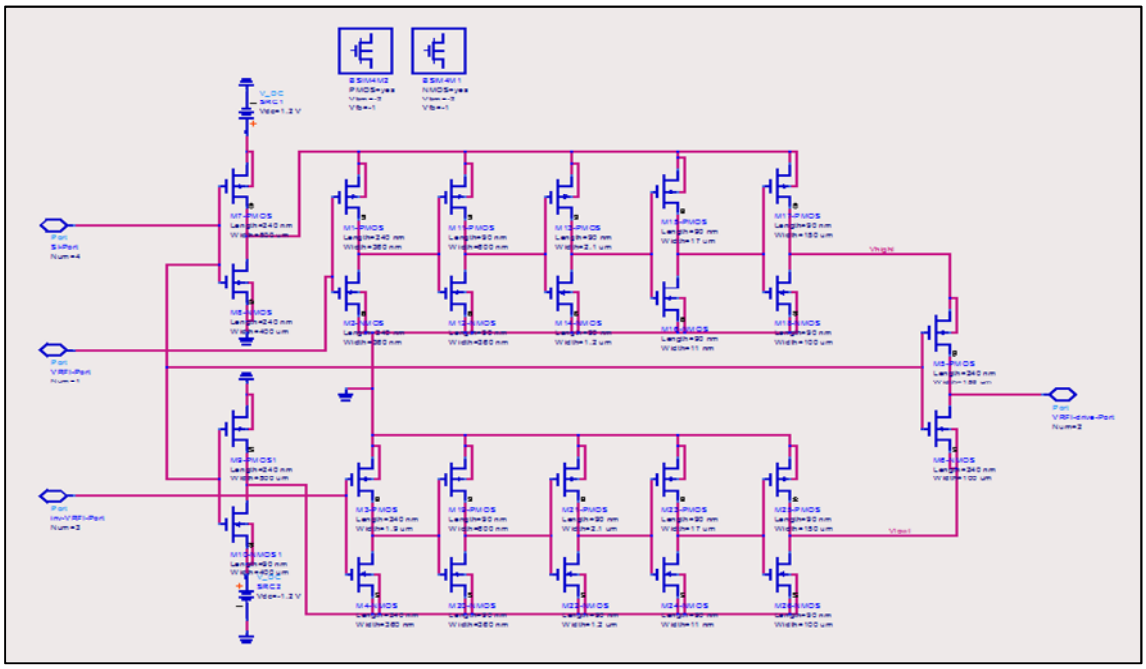


Figure (10): Driver architecture for a quadrature power amplifier

Now, The RF PA circuits involves, the QPA, driver circuit, input and output matching have been designed completely. The complete design of RF power amplifier system is explained on the block diagram shown in Figure (11). The analysis of this design can be divided in to two ways: one of these analysis in time domain response (Transient response) and other analysis in frequency domain (Harmonic response).

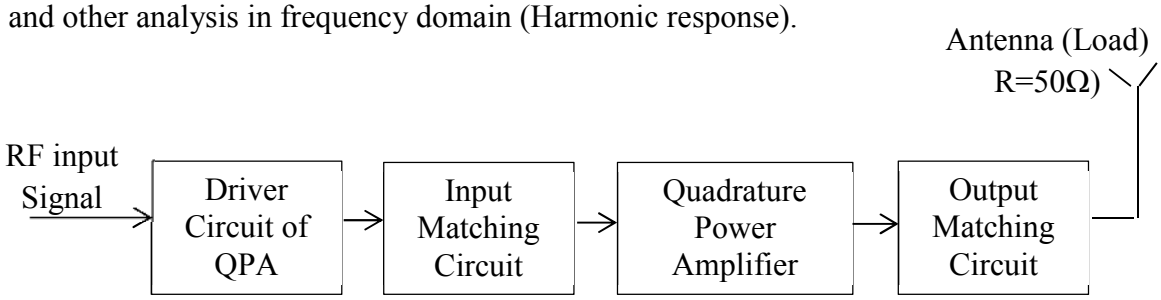


Figure (11): Block diagram of the transmitted rf signal by using QPA

4-7 Transient Simulation

A transient simulation will be performed to check the quadrature PA's functionality. The quadrature signals I(t) and Q(t) will be set as sinusoid with 90º phase difference. These signals performed at massage frequency f_{IQ}=50MHz. The function of parity bit signals SI(t), SQ(t) which are generated from quadrature signals I(t) and Q(t) respectively. The driver circuit of QPA which contain a sets of switches function to supply rails for the chain of inverters as explained in Figure (10). The output signals of RF driver circuit are shown in Figure (12). It can be seen from Figure, the phase shift between two modulated signals is 90º and ripple output occurred because of the changing the size of the transistors and the effects of unbalanced driver output results in an uneven output rise and fall times for a single end

QPA. To eliminate ripples, the need for matching between an envelope and a phase paths. The complete design of the power amplifier which consists of two quadrature modulated PA, 90° phase difference in bridge mode is shown in Figure (13). The envelope at the QPA output should not be constant. At the output, the signal is filtered by LCR, resulting in a sinusoid with the same shaped. The maximum amplitude V_{out}=510mV as shown in Figure (14).

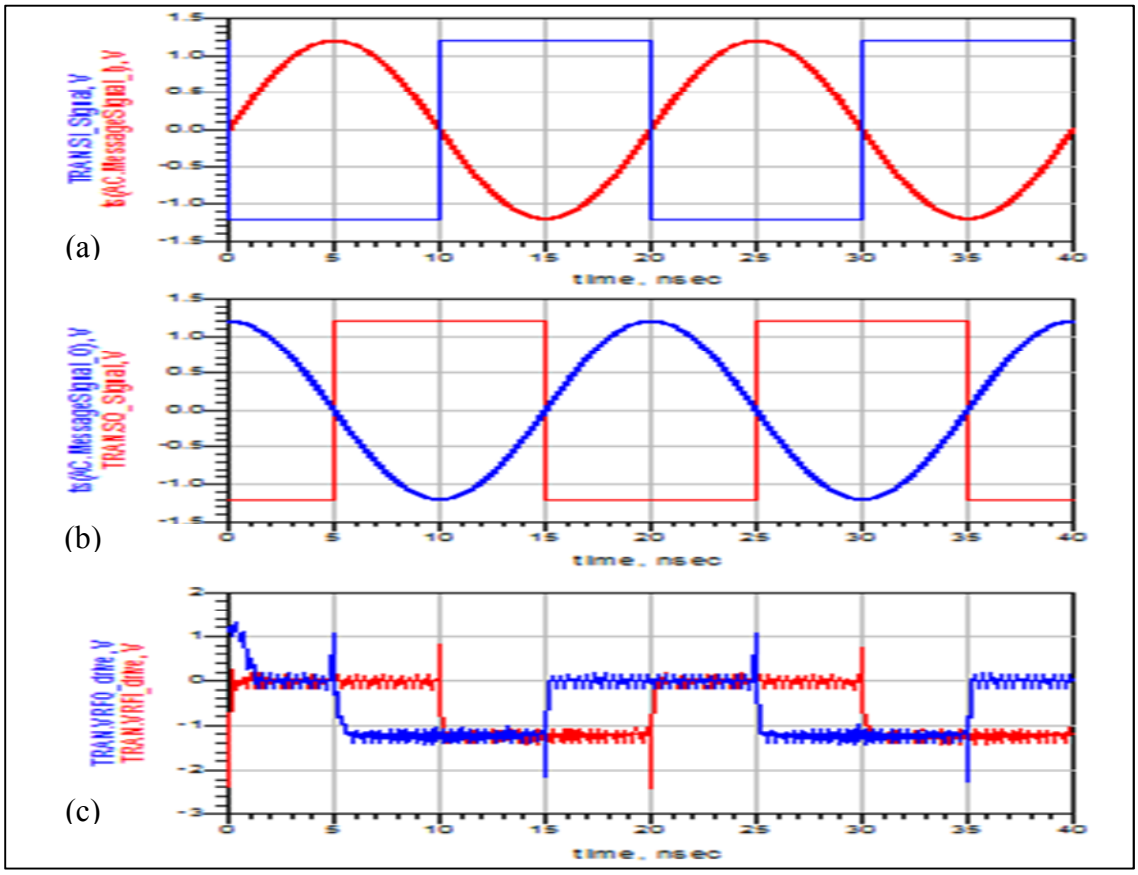


Figure (12): (a) Message signal I(t) with parity bit signal SI(t), (b) Message signal Q(t) with parity bit signal SQ(t), (c) Output signal of driver circuit for QPA

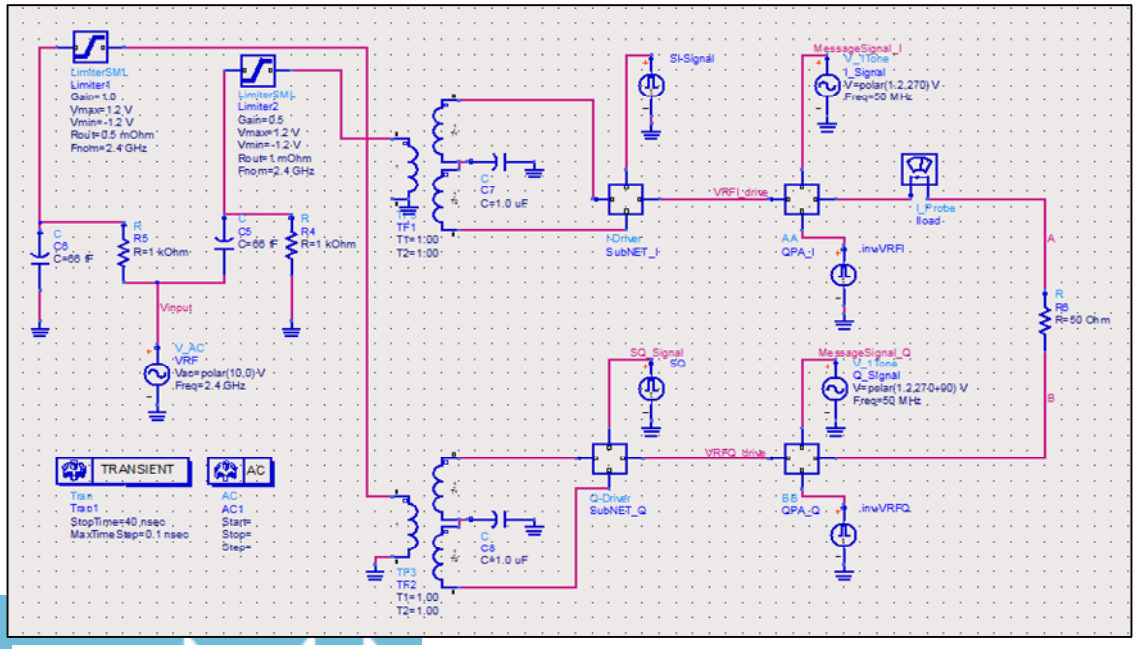


Figure (13): Full schematic design of quadrature power amplifier

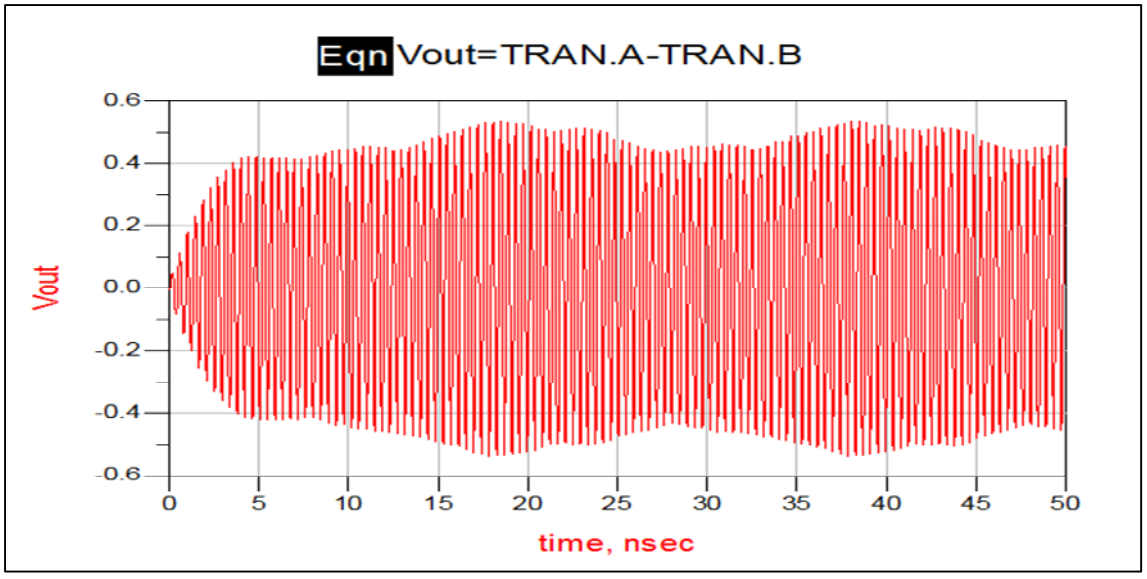


Figure (14): Simulations results for the quadrature power amplifier output with I(t) and Q(t) sinusoid At 50MHz bandwidth

4-8 Single-tone Simulation

One-tone harmonic balance simulations were performed on the QPA design. Harmonic balance is a frequency-domain analysis technique for simulating distortion in nonlinear circuits. Harmonic balance determines the spectral content of voltages and currents in the circuit. It is very useful to compute intercept point and intermodulation distortion. This is also used to determine PAE of the amplifier in the presence of interferers. Figure (15) explains the final realization of QPA design on the one tone simulation. The amplifier has very good PAE% at maximum output power (24.35dBm) as show in Figure (16). Furthermore the amplifier has high linearity and low distortion via through, see the output spectrum at fundamental frequency on Figure (17). The minimum value of amplitude and phase distortion have been obtained in this design is shown in Figure (18).

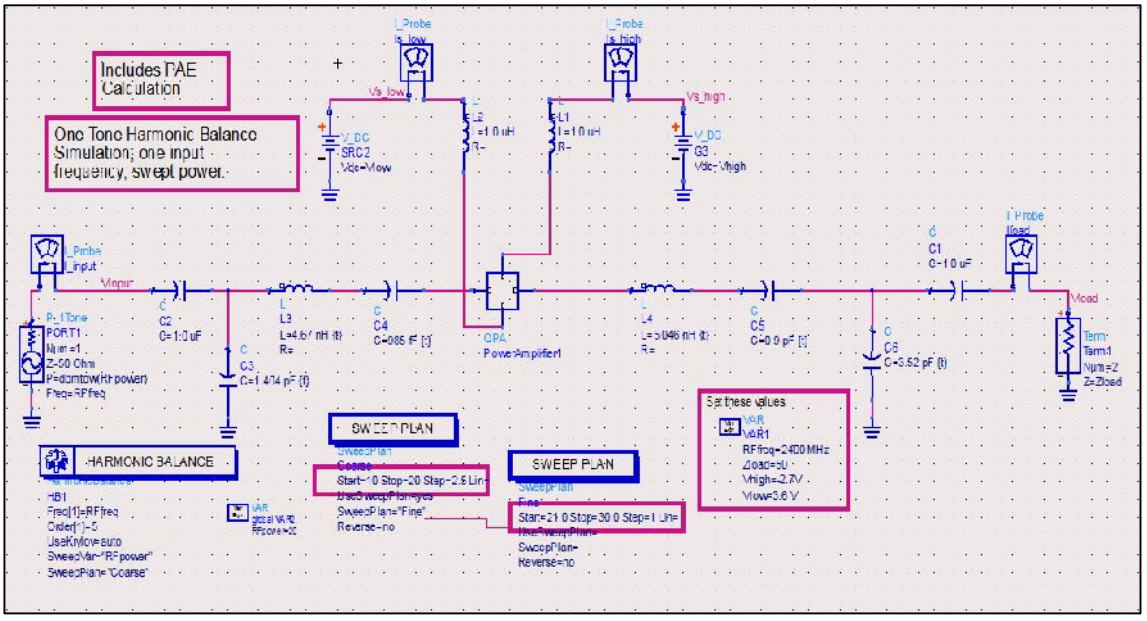


Figure (15): Schematic of the quadrature power amplifier design

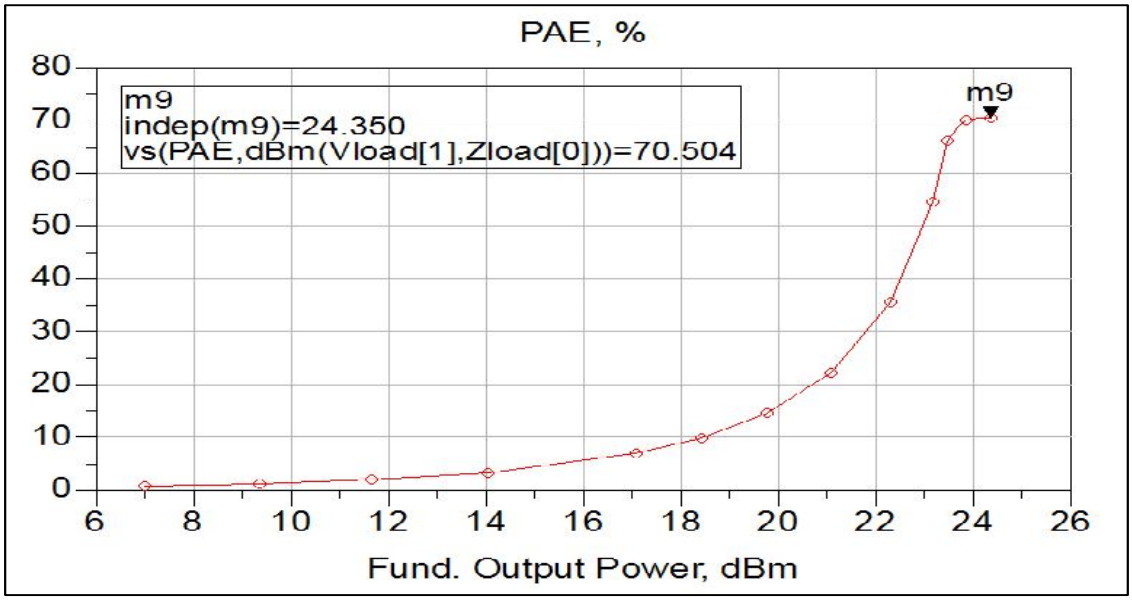


Figure (16): Power added efficiency of the qpa designed at max. Output power

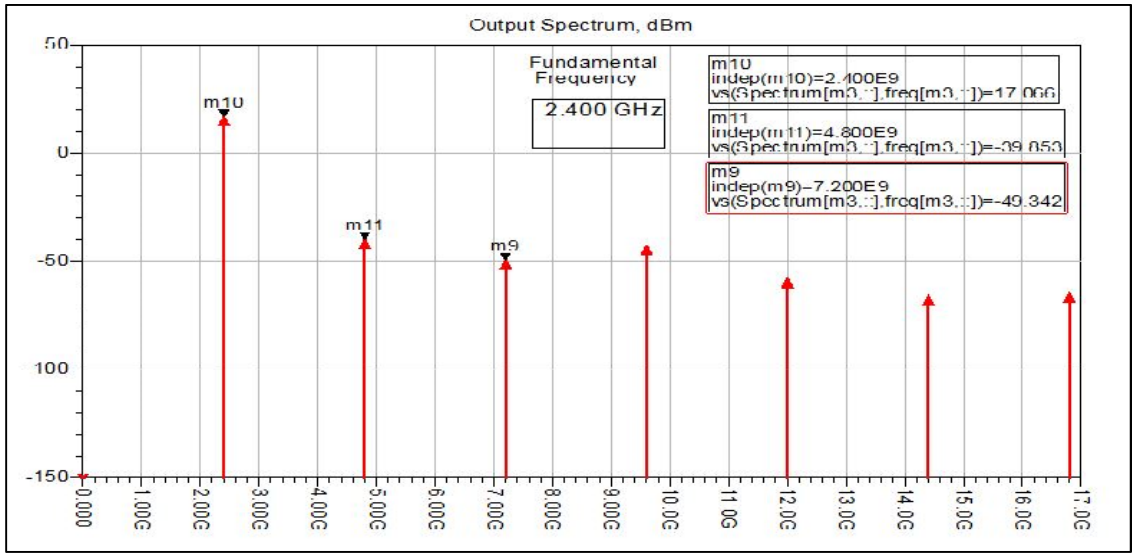


Figure (17): Output spectrum of the qpa designed when IDM3 is (-62.6dBm) at maximum output power

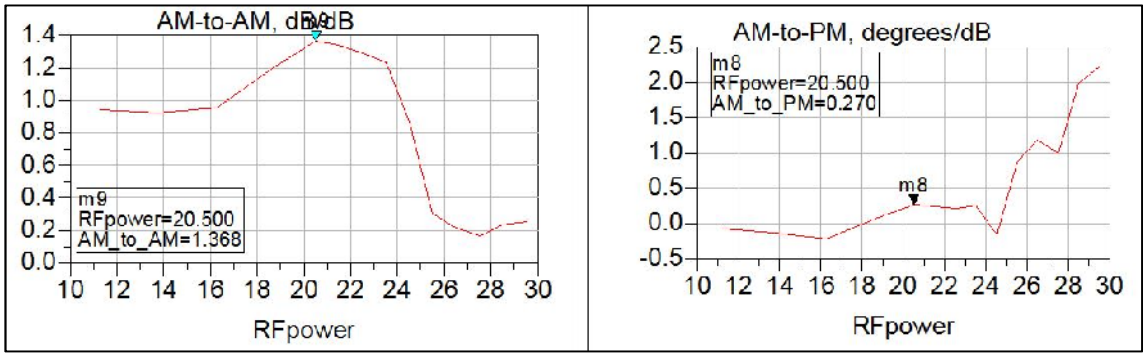


Figure (18): Amplitude distortion (AM-To-AM) and phase distortion (AM-To-PM) of the power amplifier designed at input power is greater than (20dBm)

5- Conclusion

The quadrature power amplifier and driver model is designed in 90nm CMOS technology operating at V_{DD}=1.2 V, V_{SS}=-1.2 V, was f_{RF}=2.4GHz. Besides the 90-nm feature length devices, larger devices models with a feature length of 240nm were used. The design and analysis (Time domain and frequency domain) of the quadrature power amplifier were studied at different operating frequencies. It is found that the amplifier can operate at W-CDMA base station and wireless application (WLAN) at input power level more than 20dBm. The amplifier has good efficiency about (PAE%=70.5%) at bandwidth message signals f_{IQ}=50MHz, and has good output spectrum and third harmonic spectrum is less than the main spectrum by amount of (20dBm). The third order intermodulation (IDM3) has been obtained about (-62.6dBc) at maximum output power (24.35dBm). The amplitude distortion is gotten about (1.36 dB/dB), and phase distortion about (0.27 degree/dB).

6- References

[1] A. V. Grebennikov, "RF And Microwave Power Amplifier Design", New York: McGraw-Hill, 2004.

[2] S.C. Cripps, "RF Power Amplifier For Wireless Communication", Artech House, Second Edition, 2006.

[3] Shirt Fun OOI, "Design Of A High Efficiency Class F Power Amplifier Integrated With Microstrip Antenna", Ph.D. Thesis, School Of Computing ,Engineering And Information Sciences North Umbria University At Newcastle ,2007.

[4] Andrei Grebennikov, Nathan O. Sokal, "Switch Mode RF Power Amplifiers", Burlington, MA: Elsevier, 2007.

[5] C.H. Li, "Quadrature Power Amplifier For RF Application", Thesis In Partial Fulfillment Of The Requirements For The Degree Of Master Of Science, Faculty Of Electrical Engineering, Mathematics & Computer Science, University Of Twente, Netherlands, November 2009.

[6] F. Wang And Others, "Wideband Envelope Elimination And Restoration Power Amplifier With High Efficiency Wideband Envelope Amplifier For WLAN 802.11g Applications", IEEE MTT-S Int. Microw. Symp. Dig., pp. 645-648, Jun, 2005.

[7] I. Kim And Others, "High Efficiency Hybrid EER Transmitter Using Optimized Power Amplifier", IEEE Transactions On Microwave Theory And Techniques, vol. 56, no. 11, pp. 2582-2593, Nov., 2008.

[8] B. Taurkel And M. Fatih, "Linearized 2.4-GHz Power Amplifier", Progress In Electromagnetics Research Symposium Proceedings, KL, MALAYSIA, March 27-30, P.1389-1392, 2012.

The work was carried out at the college of Engineering. University of Mosul